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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,068	02/13/2004	Kyoji Yamashita	60188-773	5633

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EXAMINER
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ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,068	YAMASHITA ET AL.	
	Examiner	Art Unit	
	Anjan K. Deb	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Rogers (US 6,838,869 B1).

Re claim 1, Rogers discloses semiconductor device (Fig. 13) (col. 24 lines 64-67, col. 8 lines 1-20) having first conductor member (Electrode A), a second conductor member (Electrode B), provided with a dielectric (C_{AB}) interposed between the first conductor member and the second conductor member, a third conductor member (Electrode C), provided with a dielectric interposed (C_{AC}, C_{BC}) between each of the first and second conductor members and the third conductor member, and a capacitance measuring circuit (Fig. 1), wherein the capacitance measuring circuit comprises a charging voltage supply part (1357) for charging the first conductor member (Fig. 13), said charging voltage (bias voltage) supply part being connected via a first charge-side switching transistor (see for example switching transistors 102,105)(Fig. 1) to the first conductor member, a current sampling part for sampling currents flowing through the second and third conductor members (col. 7, lines 61-67, col. 8 lines 1-20), said current sampling part being connected via first and second switching transistors for measuring current to the second and third conductor members, respectively, and a control circuit (ON CHIP Control

Circuitry)(Fig. 5) for controlling ON/OFF switching of each of the switching transistors (102, 104), and the second conductor member is connected to the charging voltage supply part via a second charge-side switching transistor whose ON/OFF switching is controllable by the control circuit.

Re claim 8, Rogers discloses the first through third conductor members may comprise interconnects such as the capacitance associated with interconnects metal (col. 14, lines 22-26).

Re claims 9, 10 Rogers discloses first through third conductor members are any three-way combination source/drain region, a substrate region and a gate electrode of a MISFET (MOSFET)(Fig. 13) having three electrode structure. Re claims 8,9 MISFET or NMISFET are broadly interpreted as MOSFET having P-well or N- well located in the substrate region (Fig. 22).

3. Claims 1, 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 6,300,765 B1).

Re claim 1, Chen discloses semiconductor device (Fig. 1)(104) (col. 24 lines 64-67, col. 8 lines 1-20) having first conductor member (105), a second conductor member (106-n), provided with a dielectric (C_n) interposed between the first conductor member and the second conductor member, a third conductor member (106-N), provided with a dielectric interposed (C_N) between each of the first and second conductor members and the third conductor member, and a capacitance measuring circuit (112,113,133,138,131), wherein the capacitance measuring circuit

comprises a charging voltage supply part (I_{CHRG1})(I_{CHRG2}) for charging the first conductor member, said charging voltage supply part being connected via a first charge-side switching transistor (119)(112) to the first conductor member, a current sampling part for sampling currents flowing through the second and third conductor members (106-n), said current sampling part being connected via first and second switching transistors (112) for measuring current (A)(138) and a control circuit (121,122,116,115) for controlling ON/OFF switching of each of the switching transistors (112, 113), and the second conductor member is connected to the charging voltage supply part via a second charge-side switching transistor whose ON/OFF switching is controllable by the control circuit.

Re claim 8, Chen discloses first through third conductor members (105, 106-1, 106-n, 106-N) are interconnects (see abstract, line3, "interconnect capacitances").

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 5-7, 11, 13,14 rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers (US 6,838,869 B1).

Re claims 2, 5-7, Rogers did not explicitly disclose third conductor member is connected via third charge-side switching transistor to charging voltage supply part, and the first conductor member is connected via a third switching transistor for measuring current but would have obvious in view of the switching transistors switching transistor (102, 104) (Fig. 1) disclosed by Rogers for measuring the capacitance 110.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Rogers by adding third switching transistor for charging and measuring capacitance in three electrode capacitor structure.

Re claim 6, Rogers discloses switching transistors comprising MOSFET, which are broadly interpreted as MISFET or NMISFET.

Re claim 11, Rogers discloses that the method of measuring capacitance of three-electrode system (Fig. 13) can be extended to capacitors with more than three electrodes (col. 24 lines 64-67, col. 25 lines 1-20).

Rogers did not expressly disclose fourth conductor connected to fourth switching transistor.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Rogers by adding fourth switching transistor for charging and measuring capacitance in four electrode capacitor structure.

Re claim 13, Rogers did not explicitly disclose oscillator for generating a clock signal having a higher frequency than an external clock signal, but would have obvious because Rogers disclosed that that the test frequency can be set low or high depending upon the application.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Rogers by adding oscillator for generating clock signal having a higher frequency than an external clock signal so that the test frequency for measuring capacitance can be set high or low depending upon the application

Re claim 14, Rogers disclosed capacitance-measuring circuit (Fig. 5) comprises a frequency divider 508 for dividing the frequency of the clock signal output from the oscillator so as to monitor frequency with standard hardware.

Allowable Subject Matter

6. Claims 3,4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 3,4 are allowable for the inclusion of switching transistor for decreasing off-leakage current placed between each of the first through third conductor members and the current

sampling part, said switching transistor being connected in series with a corresponding one of the first through third switching transistors for measuring current and having a higher threshold voltage than said corresponding switching transistor for measuring current.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Belluomini et al. (US 6,731,129) disclose apparatus for measuring capacitance of a semiconductor device comprising pair of transistors which are turned on and off alternately, with one transistor being arranged to charge the semiconductor device to a known voltage, and the other transistor being arranged to discharge the semiconductor device to zero voltage. The discharge current is monitored to provide a measure of the capacitance of the semiconductor device.

Fried (US 6,624,651 B1) discloses circuit for measuring capacitance of a structure (C_{Test}) comprising charging (applying voltage) and discharging the capacitor with switching transistors controlled by control circuit and analyzing the current that passes into the capacitive structure in the capacitance testing circuits (Fig. 1,2).

Cooke et al. (US 5,677,634) discloses apparatus for testing capacitance components by charging the component with a voltage and measuring leakage current.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lefkowitz Edwards can be reached at 571-272-2180.

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3/29/05

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